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PLEASE DELIVER TO EXAMINER JOHN B. VIGUSHINDocket No. END919910022R (IEN-10-5342-R)

Applicant(s):

Serial No.	Filing Date	Examiner	Group Art Unit
<u>09/004,524</u>	<u>January 8, 1998</u>	<u>J. Vigushin</u>	<u>1326</u>

Invention:

IC CHIP ATTACHMENT

I hereby certify that this Reply to Supplemental Examiner's Answer is being transmitted via facsimile to the United States Patent and Trademark Office

Fax. No. 703-872-9306 on February 18, 2005 10
(Date) (No. of pages)

TO: Examiner Vigushin

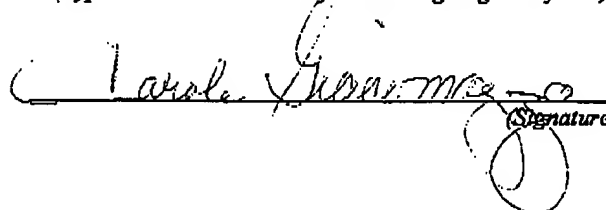
Attached is a Reply to Supplemental Examiner's Answer which was issued on January 4, 2005.

It is not believed that any fees are required. However, the Commissioner is hereby authorized to charge payment of fees associated with this communication, or credit any overpayment, to Deposit Account No. 09-0457.

FROM: William N. Hogg
CUSTOMER NO. 26681

Carole Giacomazzo

(Typed or Printed Name of Person Signing Certificate)


(Signature)

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Gedney et al)	
)	
Serial No. 09/004,524)	
)	
Filed: January 8, 1998)	Examiner: J. Vigushin
)	
For: IC CHIP ATTACHMENT)	Art Unit: 2841
)	
Reissue of U.S. Patent No. 5,483,421)	Confirmation No. 1326
)	
Attorney Docket No. IEN-10-5342-R)	
(END919910022R))	

REPLY TO SUPPLEMENTAL EXAMINER'S ANSWER

Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Appellants are replying to the Supplemental Examiner's Answer responsive to the Remand to the Examiner by the Board of Patent Appeals and Interferences, which Supplemental answer was issued under date of January 4, 2005. The examiner found that the *Eggert* case was distinguishable, and continued his rejection under the recapture doctrine. Applicants respectfully disagree with this position for the reasons enumerated below.

Appellants filed for a broadening reissue of Patent 5,483,421. The examiner rejected newly added claims 21-25 and 34 under 35 USC § 251 based on the recapture doctrine. Appellants appealed this rejection to the Board of Patent Appeals and Interferences, which, in a decision mailed July 31, 2003, remanded the case to the examiner for a determination of whether the decision holding the recapture doctrine applied, and remained appropriate in view of *Ex parte*

Eggert, decided by the Board as Appeal No.2001-0790. (Although not required, the allowed reissue claims are attached as an Appendix.)

The examiner, in a Supplemental Examiner's Answer, held "Because reissue Claims 21-25 and 34 omit the surrender-generating limitations of Elements X and Y, and fail to include a broadened replacement limitation of the area of surrender, *Pannu*, *Hester* and *Clement* are on point, while *Eggert* is not, and claims 21-25 and 34 impermissibly recapture what was previously surrendered." (emphasis original) For reasons stated *infra*, Appellants disagree with the examiner's holding, and believe that *Eggert* is on point. Therefore, it is requested that the Board reverse the examiner and allow the reissue application with claims 21-25 and 34 therein.

The examiner, in analyzing the claims states as follows:

5. In the present instance, the original independent Claims 1 and 7, which were rejected in the original Application '467 by Examiner Sparks based on prior art, did not contain:

Element X: "glass filled epoxy"

Element Y: "having a coefficient of thermal expansion of at least 17×10^{-6} ppm/ $^{\circ}$ C;"

Element Z: "an encapsulation material encapsulating said first set of solder connections;"

6. To overcome the first prior art rejection against the independent claims, the Applicant rewrote those claims to add Elements (limitations) X, Y and Z. Following the second prior art rejection, Applicant argued that the newly cited references also did not teach the concept, particularly having the three added Elements X, Y and Z. In its decision, the Board agreed with the Appellant and further supported Appellant's argued grounds for patentability, most particularly regarding Element Y. (See Board decision in application 07/848,467, Paper No. 16, June 14, 1995 at pages 5-8). Presently, on reissue, it is the present and previous Examiners' position that the Applicant is not permitted to completely delete the added limitations X and Y, whose argument of criticality by the Applicant was accepted by the Board in the original Application '467. The Applicant made the choice of adding and relying upon Elements (limitations) X, Y and Z. The Applicant chose not to prosecute variations of the original claims not including Elements (limitations) X, Y and Z.

First, it is noted that, just as in the *Eggert* case, the examiner has not rejected the claims under 35 U.S.C. §§ 101, 102, 103, or 112. Therefore, the only issue that needs to be determined is whether claims 21-25 and 34 are barred by the recapture doctrine under 35 U.S.C. § 251. It is submitted that they are not barred and, therefore, allowance of these claims is respectfully requested.

Initially, it should be noted that the Board in *Eggert* used a concentric circle diagram to explain the recapture doctrine. This diagram, referred to as diagram 1, is as follows:

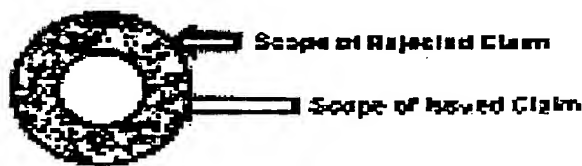


DIAGRAM 1

In describing the diagram, the Board made the following holding:

For example, if an outer circle claim contains elements ABC and the inner circle claim contains elements ABCDEF, a reissue applicant cannot recapture a claim directed to elements ABC (outer circle) or a claim entirely outside the outer circle (e.g., AB, BC, ABC_{BR}², etc.). However, it is our view that the reissue recapture rule is not invoked for claims directed to elements ABCX, ABCD_{BR}, ABCEF, A_{BR}BCDEF. In other words, the focus for determining the reach of the reissue recapture rule should be the claim from which the issued claim directly evolved, not the issued claim itself. We believe that this is where we and the members of the dissent disagree.

Thus, the Board held that claims of the same or broader scope than ABC are subject to the recapture rule, but claims narrower than ABC in any way are not subject to the recapture doctrine. In other words, a claim that falls into the shaded zone between the concentric circles is *not* subject to the recapture doctrine. See section of *Eggert* decision bridging pages 3 and 4 as:

The shaded area between the circles represents subject matter which is only narrower than the scope of the rejected claim but only broader than the scope of the issued claim. In our view, the surrendered subject matter is the outer circle of Drawing 1 because it is the subject matter appellants conceded was unpatentable. The subject matter of the shaded area was not subject to the administrative examination process as the

examiner was never directly presented with a claim which fell within the scope of the shaded area. Thus, appellants have never conceded that a claim falling within the scope of the shaded area of Drawing 1 is unpatentable and therefore, in our view, such subject matter is not barred by the recapture rule.

Thus, it appears that the examiner is equating his use of X, Y, and Z to the Board's use of D, E and F. In such a case, the holding of the Board in the above quoted section unequivocally indicates that claims 21-25 and 34 are clearly allowable, since while the claims are broader in some respects than the issued claim, they are narrower in some respects than the rejected claims.

Another way of looking at the claims is that the terms "glass filled epoxy" and "having a coefficient of thermal expansion of at least 17×10^{-6} ppm/°C" as limitations to the characteristics of the chip carrier, and the elimination of these terms is, in fact, broadening the term "chip carrier" and, thus, this would be analogous to A_{BR}BCDEF of *Eggert*. However, this also is within the shaded zone between the concentric circles and, thus, is *not* subject to the recapture doctrine. Indeed, this is a better way to view the claims. In fact, when viewed this way, the examiner's rationale for the non-applicability of *Eggert* is completely non-applicable. The examiner states:

It is to be noted that the Board focused on the Element Y limitation argued by the Applicant to define over the prior art rejection. However, the Element X limitation goes hand-in-hand with the Element Y limitation. Thus the two critical limitations were **deleted in their entirety**; whereas, in *Eggert*, the critical limitation was **retained in broadened form**. (emphasis original)

Also, in the *Eggert* case, the Board held, at page 21, "Ball also establishes that '[t]he proper focus is on the scope of the claims, not on the individual feature or element purportedly given up during the prosecution of the original application.'" (emphasis original) Hence, in view of all of this, it is clear that the recapture doctrine does not apply, and all of the claims in the reissue application should be allowed.

The Board also distinguished the *Eggert* case over various other cases which held the recapture doctrine applied. In this, the Board seems to be pointing out that the more limiting aspect of the claim has to relate to the broadening of the claim, and the examiner takes the position that:

Further, as stated by the present Examiner in his Final Action (see the last five lines on p.3 of Paper No. 7), the Element Z, "was not considered to be germane to the prior art rejection given in Application '467." In this instance, there is no apparent replacement narrowing limitation that relates to and is a broadened version of the omitted surrender-generating limitations (Elements X and Y), which pertain to the material of the chip carrier and the coefficient of thermal expansion of that material.

However, it is clear that the encapsulation limitation (Element Z) is intimately related to the **composition** and the CTE as stated in the declaration of Mr. Gedney, one of the inventors, who states as follows:

...was conceived when he and the aforesaid Tamar A. Sholtes, his co-inventor, were members of a team at IBM's Endicott facility working on direct chip attachment. We realized that recent developments in encapsulation technology had made it possible to mount integrated circuit chips on chip carriers with higher coefficients of thermal expansion ("CTEs") than previously thought possible. These developments allowed us to consider building chip carriers out of organic dielectric materials such as glass-filled epoxies (commonly referred to as FR-4 materials) frequently used for printed circuit board or cardstock, or polyamides frequently used in tape automated bonding.

And reinforced by the undersigned's declaration:

It is also not obvious from the cited references that an IC chip with fine line conductors, e.g. 0.001 inch wide and bond pads spaced close together, e.g. 0.008-0.010 inch apart, could be successfully connected to a printed circuit board having wires at least 0.005 inches wide and bond pads spaced at least 0.050 inch apart by bonding the chip to an organic chip carrier having a CTE significantly higher than the CTE of the chip, encapsulating the solder connections between the chip and carrier to absorb or reduce thermally induced stresses in these connections, and bonding the chip carrier to a circuit board made of the same organic material or another with a similar coefficient of thermal expansion. As noted above and at column 8, lines 17-45 of the '421 patent, this produces a number of very significant advantages. Neither these advantages, nor the structure and methods by which applicants produce them are disclosed or suggested by the cited references.

Thus, far from being non-related to the X and Y limitation broadening, the narrowing Z limitation is the *sine qua non* of the underlying ability to make these changes. Hence, even under this restrictive interpretation, the recapture rule clearly does not apply.

CONCLUSION

In view of the above, it is requested that the examiner's rejection of the reissue claims be reversed, and that claims 21-25 and 34 be allowed.

Respectfully submitted,

Date: 2-18-05



William N. Hogg, Reg. No. 20,156

DRIGGS, LUCAS, BRUBAKER & HOGG CO., L.P.A.
CUSTOMER NO. 26681

WNH:cg

Attachment

APPENDIX

21. A package mounting integrated circuit chips onto a circuit board comprising:
- an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;
 - a chip carrier formed of an organic dielectric material having first and second opposite surfaces;
 - a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;
 - a pattern of conductors on said chip carrier connected to accommodate said input/output pads;
 - a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;
 - an encapsulation material encapsulating said first set of solder connections;
 - a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;
 - electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;
 - a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;
 - a set of electrical connection sites formed on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and
wiring on said circuit board connected to said second set of bonding pads.

22. A package according to claim 21 wherein the thermal coefficient of expansions of the material of the chip carrier and the material of the circuit board do not differ by more than about 20%.

23. The package of claim 21 wherein said chip carrier and said circuit board are formed of the same material.

24. A package according to claim 21 wherein said chip carrier is formed of a glass filled epoxy.

25. A package according to claim 21 wherein said chip carrier is formed of a polyimide.

34. A method of mounting integrated circuit chips onto a circuit board comprising:
providing an integrated circuit chip having a surface array of input/output pads on one side thereof which array forms a footprint;

providing a chip carrier formed of an organic dielectric material having first and second opposite surfaces;

forming a first set of bonding pads formed on said first surface of the chip carrier and arranged in an array corresponding with the chip footprint;

providing a pattern of conductors on said chip carrier connected to accommodate said input/output pads;

forming a first set of solder connections interconnecting the input/output pads on the chip to said first set of bonding pads on the chip carrier;

encapsulating said first set of solder connections;

forming a second set of bonding pads formed on the second surface of the chip carrier arranged in an array;

forming electrically conducting vias extend through the chip carrier connecting said first set of bonding pads to the second set of bonding pads;

providing a circuit board formed of an organic material having a coefficient of thermal expansion similar to the chip carrier;

forming a set of electrical connection sites on said circuit board and arranged in a pattern corresponding to the pattern of the array of the second bonding pads on said chip carrier;

forming a second set of solder connections interconnecting the pads of said second set of bonding pads on the chip carrier to the connection sites on the circuit board; and

forming wiring on said circuit board connected to said second set of bonding pads.